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10/807,446	03/24/2004	Hisakazu Date	XA-10062	3358

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EXAMINER	
RADOSEVICH, STEVEN D	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 06/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/807,446	DATE, HISAKAZU	
	Examiner	Art Unit	
	Steven D. Radosevich	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2004* & 8/4/04.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☒ Claim(s) *1,5,7,12,15 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-17 are present for examination.

Priority

Acknowledgement is made that foreign priority is claimed for this application and as such the date (03/31/2003) is being used for this examination.

Information Disclosure Statement

Acknowledgement is made that an Information Disclosure Statement (IDS) was provided with the application.

Drawings

The drawings are objected to because descriptive labels other than numerical are needed for figures 1, 2, 5, 6, 10, and 11. See 37 CFR 1.84(o). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance. Other objections or the specific descriptive labels required in the drawings are as follows:

Figure 1 has two different elements with numerical identification "22" and it appears that one of the elements with the numerical identification "22" is lacking an essential input that would allow selection of one of its two inputs.

Figure 2 requires more then a numerical identification for element 12 since it is unclear what is being illustrated here.

Figures 5 and 6 require more then a numerical identification for elements 1001-1004 to clearly identify what logic components are being illustrated.

Figure 10 as in figure 1 appears to have an element (38) lacking an essential input that would allow selection of one of its two inputs.

Figure 11 requires more then numerical identification of the different blocks illustrated for a clear understanding.

Appropriate correction is required for all the figures to overcome the objections.

Claim Objections

Claims 1, 5, 7, 12, 15, and 17 are objected to because of the following informalities:

Claims 1 and 7 in line 3 of the claim does not end with the appropriate semicolon after "combination circuit."

Claims 5,12, 15, and 17 in line 2 does not end with the appropriate colon after "further comprising."

Claim 12 in line 4 of the claim does not end with the appropriate semicolon after "clock buffer."

Appropriate correction is required to overcome the Objections.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 6 rejected under 35 U.S.C. 102(b) as being anticipated by Nagata Eiji (JP2002076123) as stated within Applicant Admitted Prior Art (AAPA).

1. As per claim 6, AAPA teaches a semiconductor integrated circuit comprising:

A scan diagnosis circuit capable of performing a scan test of a circuit (page 1 line 19), wherein

Said scan diagnosis circuit includes a clock buffer, and a plurality of scan flip-flops dispersed on the area to which the clock signal is supplied form said clock buffer (page 1 lines 21 and page 3 lines 4-6); and

Said scan diagnosis circuit has a scan chain connection in the order of the scan flip-flop having the largest delay of the clock signal from said clock buffer to said scan flip-flop (page 3 lines 4-6).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-5 and 7-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants Admitted Prior Art (AAPA) and as evidenced by TIME CONSTANTS, Hasunuma et al. (6069071), Antosik et al.(6822975), and Whetsel, JR. (2001/0047499).

2. As per claim 1, AAPA teaches a semiconductor integrated circuit comprising:

A combination circuit (page 1 line 15), and

A scan diagnosis circuit capable of performing a scan test of said combination circuit (page 1 line 19);

Wherein said diagnosis circuit comprises:

A first scan chain having a plurality of scan flip-flops connected for operating in synchronization with a clock signal (page 1 lines 20-21 and page 2 lines 2-3)

A first clock buffer for supplying the clock signal in the direction opposite to the flow direction of scan test data (page 1 lines 16-18 and page 3 lines 4-6).

AAPA does not specifically teach:

Wherein

Said scan diagnosis circuit comprises:

A second scan chain placed behind said first scan chain, and having a plurality of scan flip-flops connected for operating in synchronization with the clock signal;

A second clock buffer for supplying the clock signal in the direction opposite to the flow direction of scan test data that passes through said second scan chain; and

A return path for sending scan test data output from a scan flip-flop placed at a closest position to said first clock buffer in said first scan chain to a scan flip-flop placed at a furthermost position from said second clock buffer in said second scan chain.

However those of ordinary skill in the art at the time the invention was made would recognize that wherein the scan diagnosis circuit comprises two scan chains having a plurality of scan flip-flops connected for operating in synchronization with a clock signal with a return path sending scan test data output from the first scan chain to the input of the second scan chain would have been obvious since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Gegis Paper Co. v. Bemis Co., 193 USPQ 8.*

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to make this modification in AAPA to incorporate a second scan chain path of scan flip-flops within the diagnosis circuit connected to the output of the first scan chain of scan flip-flops to implement parallel processing of data wherein the execution of parallel processing would decrease the operation and execution time of the system or to decrease the inputs required to provide input to both scan chains.

3. As per claims 2, 9, and 10, AAPA as modified teaches a combination circuit along with a scan diagnosis circuit.

AAPA as modified does not specifically teach wherein said return path is formed of a wiring finer than a wiring forming feeder line of said clock signal(s).

However it would have been obvious to one having ordinary skill in the art at the time the invention was made to reduce the wire of the return path to a finer wire than the feeder line wire of the clock signal(s) since the examiner take official notice of the equivalence of the delay created by doing so and the delay created when using delay elements, their use in the art and the selection of either known equivalent would be within the level of ordinary skill in the art. See for example "TIME CONSTANTS" on the attached 892 of this action.

Therefore one of ordinary skill in the art at the time of the invention was made would have been motivated to reduce the wire of the return path to a finer wire within the AAPA as modified to minimize the surface area required to implement the delay required when the date and clock operate in the same direction to overcome hold violations.

4. As per claim 3, AAPA as modified teaches a combination circuit along with a scan diagnosis circuit.

AAPA as modified does not specifically teach wherein the circuit has multilayered wiring with a resistance per unit length differing between layers, and said return path is formed of a wiring having higher resistance then a wiring forming a feeder line of said clock signal.

However it would have been obvious to one having ordinary skill in the art at the time the invention was made to reduce the wire of the return path to a finer wire than the

feeder line wire of the clock signal(s) since the examiner take official notice of the equivalence of the delay created by doing so and the delay created when using delay elements, their use in the art and the selection of either known equivalent would be within the level of ordinary skill in the art. See for example "TIME CONSTANTS" on the attached 892 of this action. Additionally those of ordinary skill in the art at the time the invention was made would recognize that multilayered wiring is well known. See for example "Hasunuma et al." on the attached 892 of this action.

Therefore one of ordinary skill in the art at the time of the invention was made would have been motivated to reduce the wire of the return path to a finer wire and implement multilayered wiring with a resistance per unit length differing between layers within the AAPA as modified to minimize the surface area required to implement the delay required when the date and clock operate in the same direction to overcome hold violations and to eliminate the complexity of producing wiring of different resistances on the same layer.

5. As per claims 4, 13, and 14, AAPA teaches:

An area for inserting delay elements on the scan test data path in said return path is predefined to insert said delay element in the area (page 2 lines 8-10).

6. As per claims 5, 8, 12, 15, 16, and 17 AAPA as modified teaches a combination circuit along with a scan diagnosis circuit.

AAPA does not specifically teach:

A third/fourth clock buffer for scan test, capable of delaying the output/clock signal of said first/second clock buffer; and

A selector, capable of supplying the output/clock signal of said third/fourth clock buffer instead of the output/clock signal from said first/second clock buffer at the time of scan test to said first/second scan chain.

However those of ordinary skill in the art at the time the invention was made would recognize that delaying the output/clock signal of an output/clock signal in order to supply a different output/clock signal is well know. See for example "Antosik et al." on the attached 892 of this action.

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to delay an output/clock signal in order to supply a different output/clock signal when the output/clock signal is a defective or malfunctioning output/clock signal resulting in errors when being used.

7. As per claim 7, AAPA teaches a semiconductor integrated circuit comprising:

A combination circuit (page 1 line 15), and

A scan diagnosis circuit capable of performing a scan test of said combination circuit (page 1 line 19);

Said scan diagnosis circuit comprising:

A plurality of flip-flops having a clock signal line connected (pages 1-2 lines 21-3);

A first clock buffer connected to said first clock signal line (page 3 line 4);

Wherein

Said first clock buffer supplies a first clock signal to said first clock signal line (page 3 lines 4-5);

Said plurality of first flip-flops is formed on a first virtual line extending in a first direction, having data transferred from one end to the other end of said plurality of first flip-flops at the time of scan test (page 2 lines 4-5);

Said first clock buffer is configured such that the distance from said first clock buffer to the other end of said plurality of first flip-flops is shorter than the distance from said first clock buffer to the one end of said plurality of first flip-flops (page 3 lines 4-6).

AAPA does not specifically teach:

Said scan diagnosis circuit comprising:

A plurality of second flip-flops having second clock signal line connected;

A second clock buffer connected to said second clock signal line;

Wherein

Said second clock buffer supplies a second clock signal to said second clock signal line;

Said plurality of second flip-flops is formed on a second virtual line, having data from one end to the other end of said plurality of second flip-flops at the time of scan test;

Said second clock buffer is configured such that the distance from said second clock buffer to the other end of said plurality of second flip-flops is shorter than the distance from said second clock buffer to the one end of said plurality of second flip-flops; and

Data output from the other end of said plurality of first flip-flops is input to the one end of said plurality of second flip-flops;

However those of ordinary skill in the art at the time the invention was made would recognize that wherein the scan diagnosis circuit comprises two scan chains having a plurality of scan flip-flops connected for operating in synchronization with a clock signal with a return path sending scan test data output from the first scan chain to the input of the second scan chain would have been obvious since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Gegis Paper Co. v. Bemis Co., 193 USPQ 8.*

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to make this modification in AAPA to incorporate a second scan chain path of scan flip-flops within the diagnosis circuit connected to the output of the first scan chain of scan flip-flops to implement parallel processing of data wherein the execution of parallel processing would decrease the operation and execution time of the system or to decrease the inputs required to provide input to both scan chains.

8. As per claim 11, AAPA as modified teaches a combination circuit along with a scan diagnosis circuit as described above as per claim 7.

AAPA as modified does not specifically teach wherein said combination circuit is disposed between said plurality of first flip-flops and said plurality of second flip-flips.

However those of ordinary skill in the art at the time the invention was made would recognize that disposing the combination circuit between a first and second plurality of flip-flops is well known in the art. See for example "Whetsel, JR." on the attached 892 of this action.

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to dispose the combination circuit between to first and second plurality of flip-flops of AAPA as modified to full test the combination circuit within the system.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven D. Radosevich whose telephone number is 571-272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven D. Radosevich
Examiner
Art Unit 2138

GUY LAMARRE
PRIMARY EXAMINER